Exercise. Consider a CCS process that models a 1-place buffer, i.e., a memory cell that can contain a single value: it receives the value on channel `in`, it stores it and it delivers the value on channel `out`:

$$\begin{array}{lcl} C & \stackrel{\text{def}}{=} & \mathtt{in}(x).C'(x) \\ C'(x) & \stackrel{\text{def}}{=} & \overline{\mathtt{out}}(x).C \end{array}$$

Use the C process to implement

1. An (unordered) buffer with capacity 2, with the following behavior:

$$\begin{array}{lcl} B_2 & \stackrel{\text{def}}{=} & \mathtt{in}(x).B_1(x) \\ B_1(x) & \stackrel{\text{def}}{=} & \mathtt{in}(y).B_0(x,y) + \overline{\mathtt{out}}(x).B_2 \\ B_0(x,y) & \stackrel{\text{def}}{=} & \overline{\mathtt{out}}(x).B_1(y) + \overline{\mathtt{out}}(y).B_1(x) \end{array}$$

2. A FIFO buffer with capacity 2, with the following behaviour:

$$\begin{array}{lcl} F_2 & \stackrel{\text{def}}{=} & \mathtt{in}(x).F_1(x) \\ F_1(x) & \stackrel{\text{def}}{=} & \mathtt{in}(y).F_0(x,y) + \overline{\mathtt{out}}(x).F_2 \\ F_0(x,y) & \stackrel{\text{def}}{=} & \overline{\mathtt{out}}(x).F_1(y) \end{array}$$