### 5. System issues

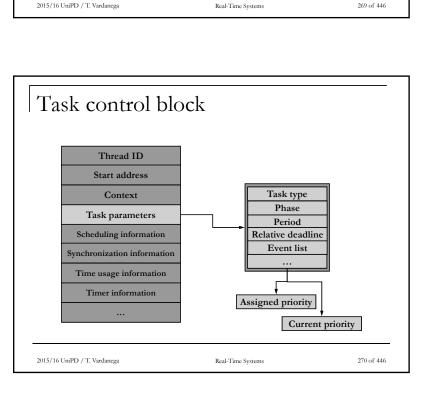
### Context switch

- Preemption causes time and space overheads which should be duly accounted for in realistic schedulability tests
- Under preemption every single job incurs at least two context switches
  - One at activation to install its execution context
  - One at completion to clean up
- The resulting costs should be charged to the job
  - Knowing the timing behavior of the run-time system we could incorporate overhead costs in schedulability tests

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Real-time operating systems /1

D Tasks are the unit of CPU allocation by the scheduler

Typically by the position assigned to tasks in the ready queue
The dispatcher gets tasks to run and operates the context switch
On task creation, some RAM is assigned to the *Task Control*

The scheduler decides which task gets the CPU

Tasks issue jobs, one at a time, which are subject to scheduling and dispatching

□ The insertion of a task in a state queue (e.g., ready) is made by placing a

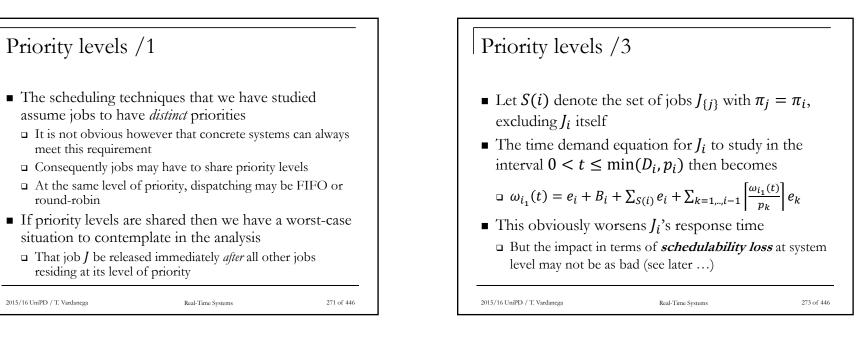
D The disposal of a task at end of life requires removal of its TCB and de-

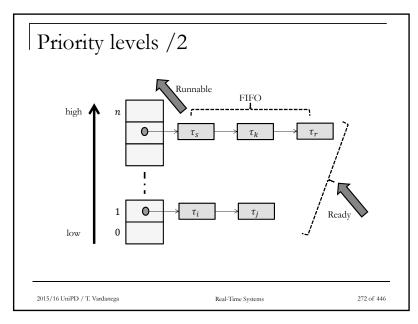
Tasks must be known to the RTOS

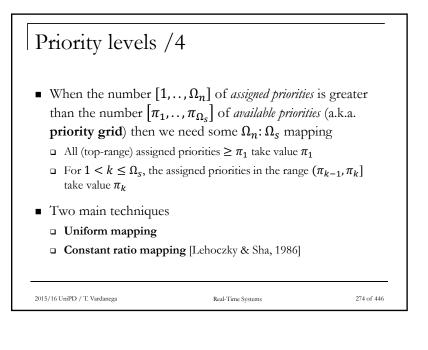
Block for that task

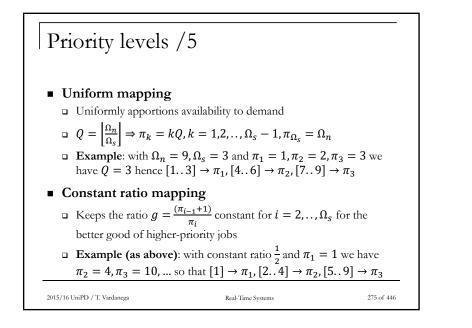
pointer to the relevant TCB

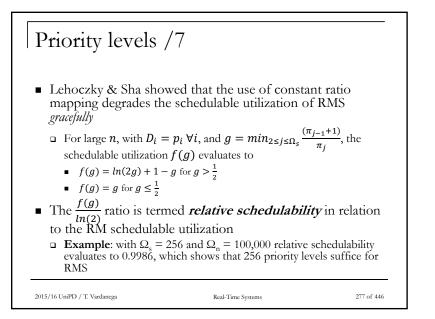
allocation of any memory it had in useIn typical embedded systems, tasks *never* terminate

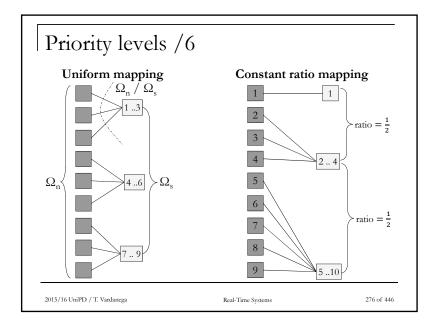


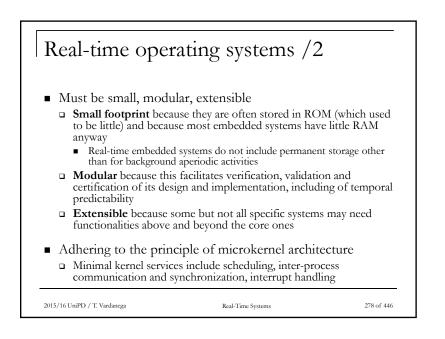


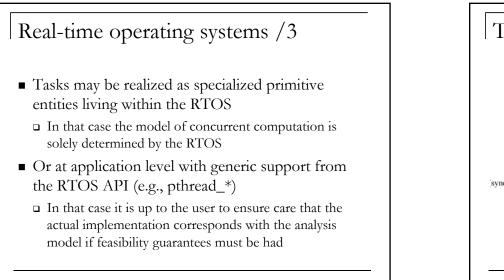








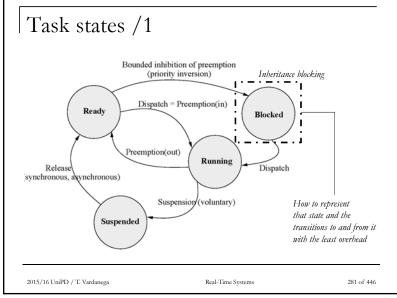


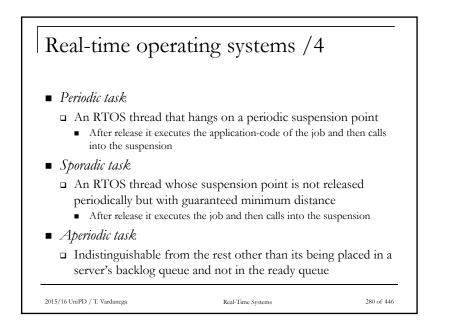




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# Task states /2 Tasks enter the *suspended* state only voluntarily By making a primitive invocation that causes them to hang on a periodic / sporadic suspension point The RTOS needs specialized structures to handle the distinct forms of suspension A time-based queue for periodic suspensions An event-based queue for sporadic suspensions But someone shall still take care of warranting minimum separation between subsequent releases (!)

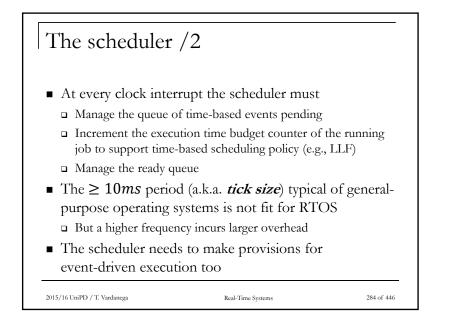
### The scheduler /1

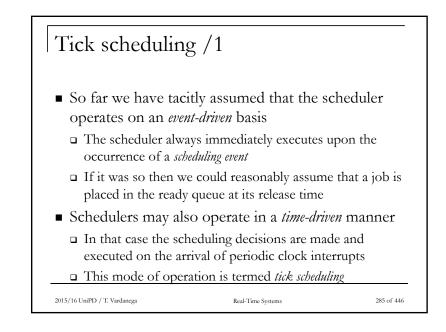
- This is a distinct part of the RTOS that does not execute in response to explicit application invocations
- It acts every time a task changes state (hence the ready queue does)
  - □ The corresponding time events are termed *dispatching points*
- Scheduler "activation" is often periodic in response to clock interrupts

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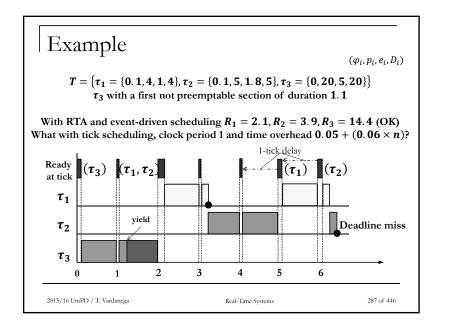
### Tick scheduling /2

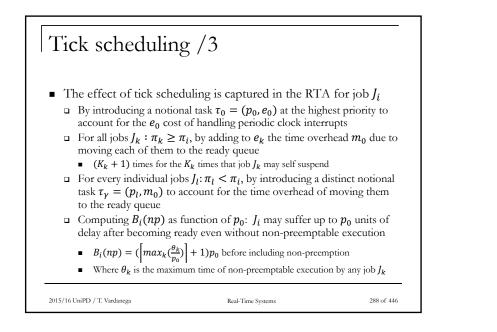
- The tick scheduler may acknowledge a job's release time 1 (scheduling) tick later than it arrived
  - □ This delay has negative impact on the job's response time
  - □ We also need to assume that a logical place exists where jobs in the "*release time arrived but not yet acknowledged*" state are held
  - □ The time and space overhead of transferring jobs from that logical place to the ready queue is not null and must be accounted for in the schedulability test together with the time and space overhead of handling clock interrupts

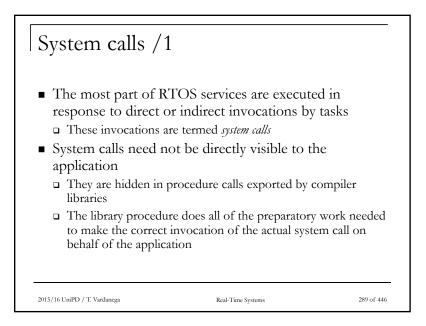
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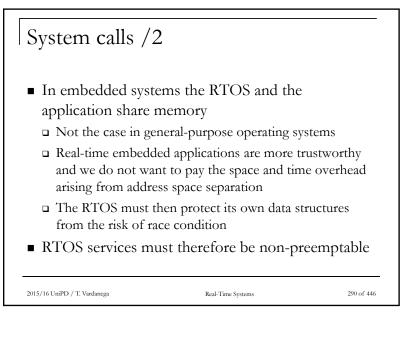
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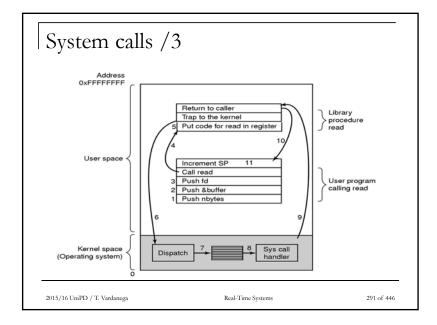
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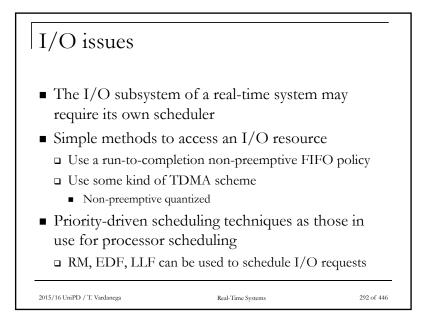


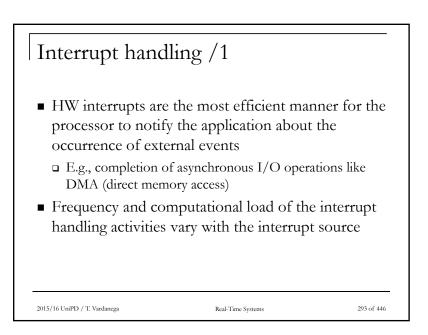


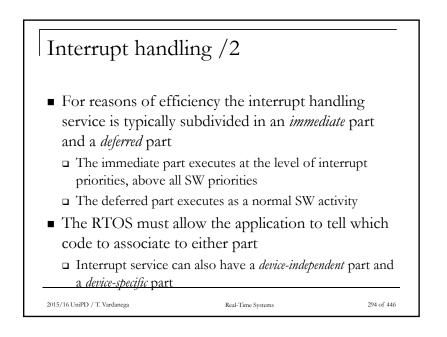






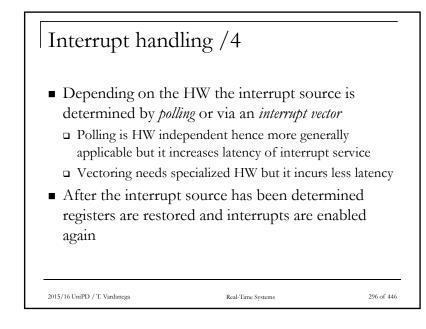


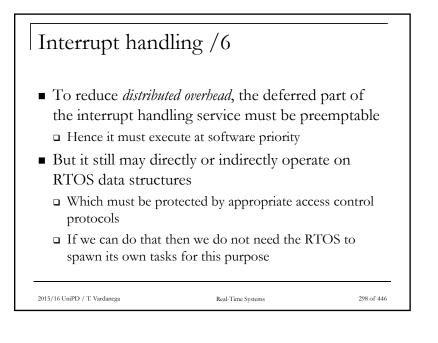




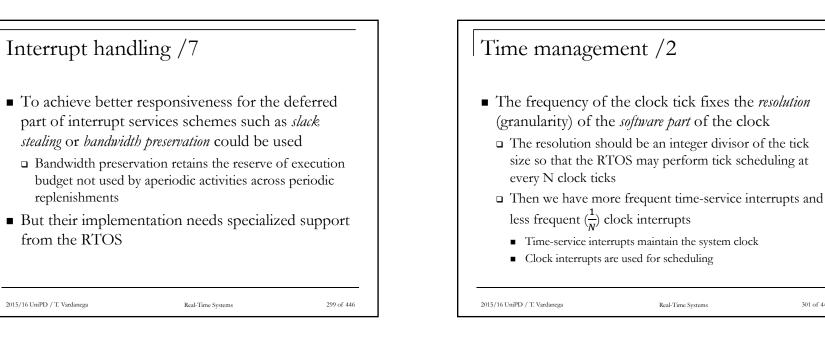
## Interrupt handling /3Interrupt he<br/>processor saves state registers (e.g., PC, PSW) in the<br/>interrupt stack and jumps to the address of the<br/>needed *interrupt service routine* (ISR)The worst-or<br/>handling is a<br/>complete to<br/>pipeline, ac• At this time interrupts are disabled to prevent race<br/>conditions on the arrival of further interrupts• Disable inter<br/>highest prior<br/>• This durat<br/>• Save the co-<br/>interrupt service is subject to scheduling2015/16 UnIPD / T. Vardanega2015/16 UnIPD / T. Vardanega

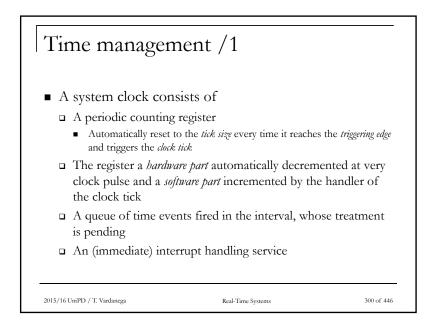
### Interrupt handling /5 The worst-case latency incurred on interrupt handling is determined by the time needed to Complete the current instruction, save registers, clear the pipeline, acquire the interrupt vector, activate the trap Disable interrupts so that the ISR can be executed at the highest priority This duration corresponds to *interference across interrupts*Save the context of the interrupted task, identify the interrupt source and jump to the corresponding ISR Begin execution of the selected ISR

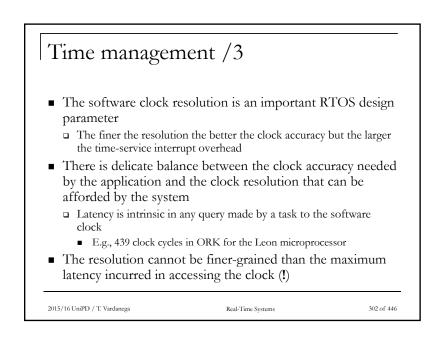




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 $TS + CS2) + I_{clock}^{R_i^n} + I_{extIm}^{R_i^n}$ 

Interference from

the clock

Interference from

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interrupts

