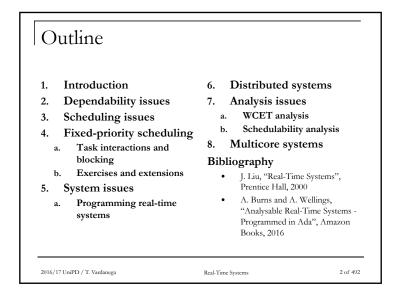
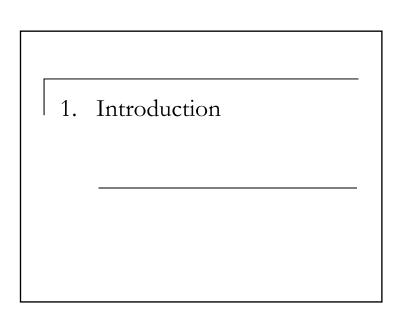
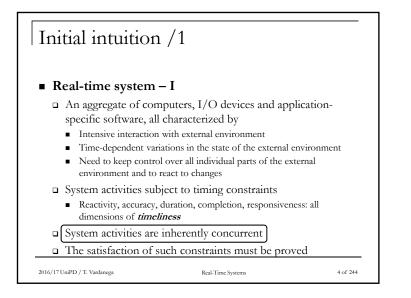
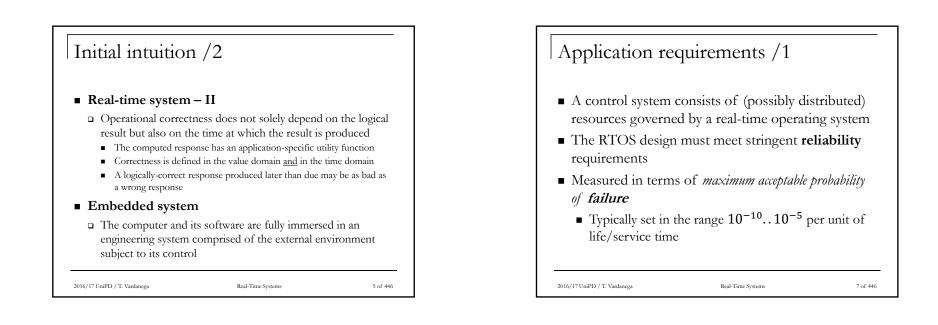
Real-Time Systems

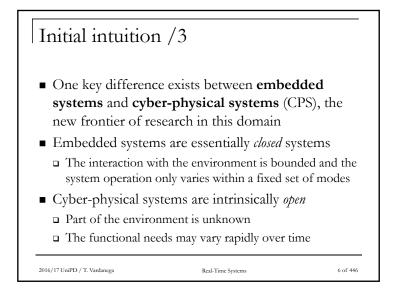
Anno accademico 2016/17 Laurea magistrale in informatica Dipartimento di Matematica Università di Padova Tullio Vardanega

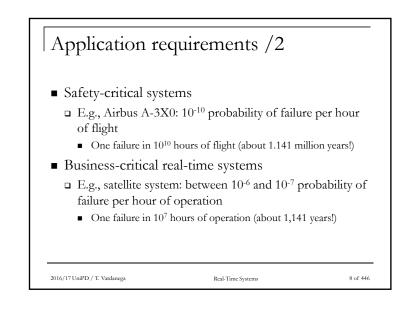


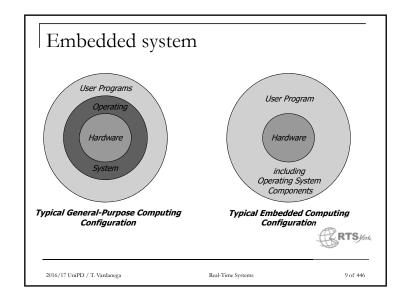


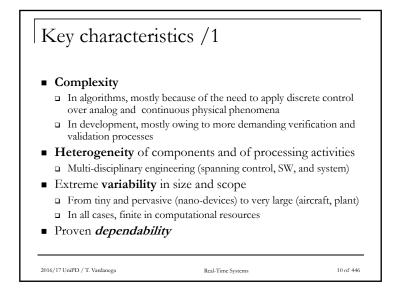


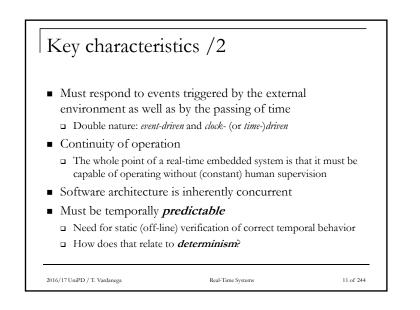


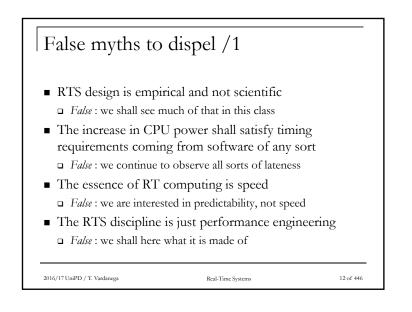






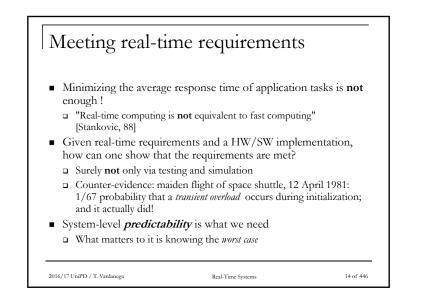


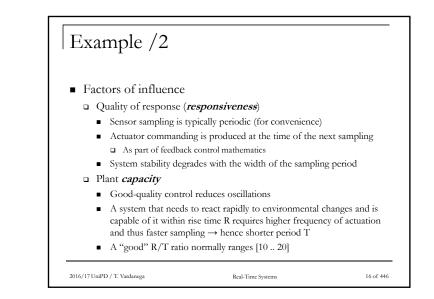


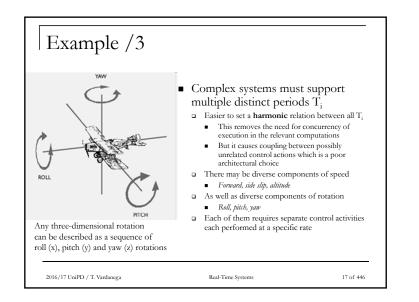


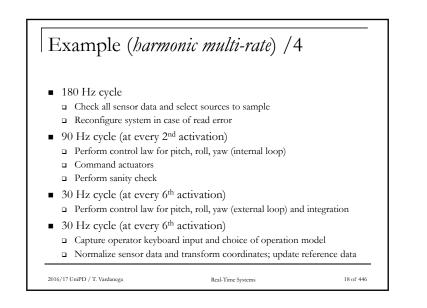
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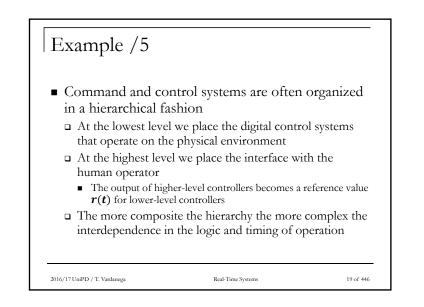


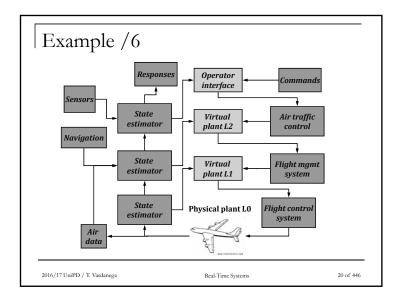


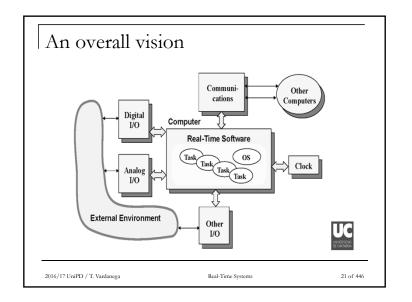


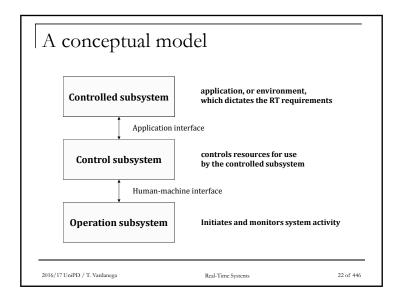


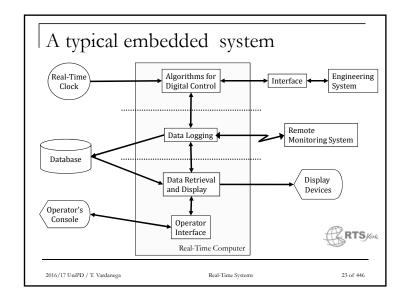


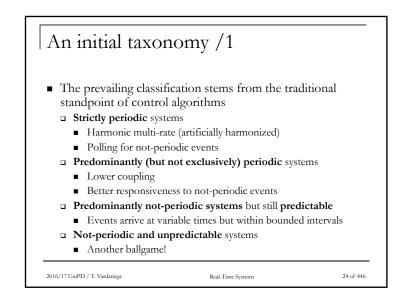


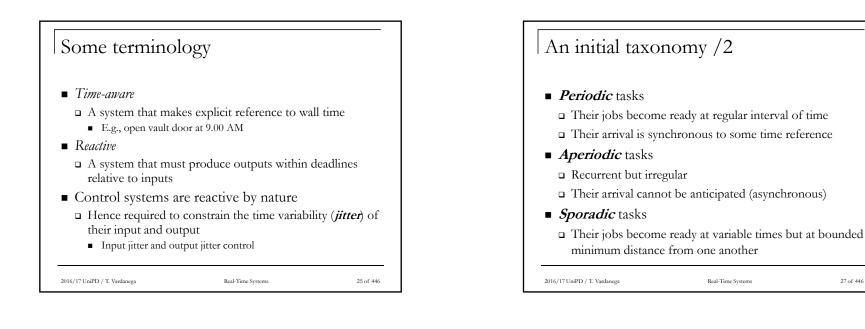


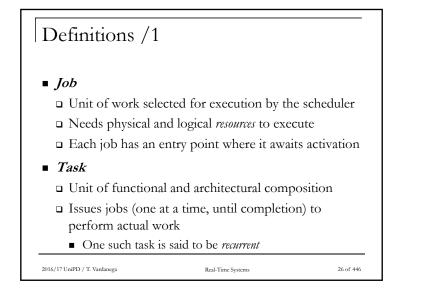


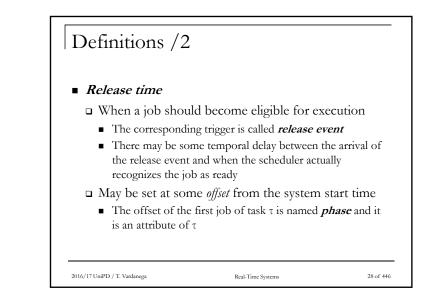


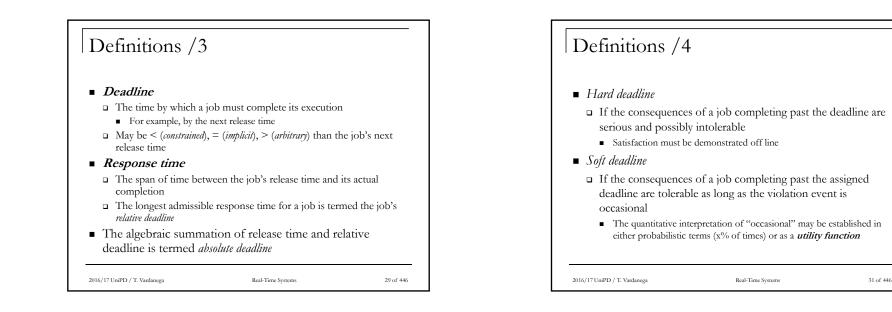


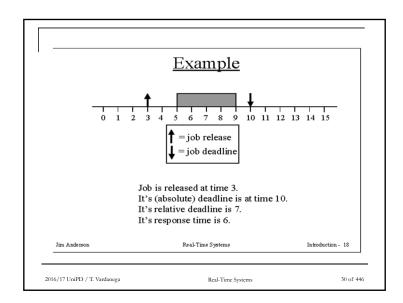


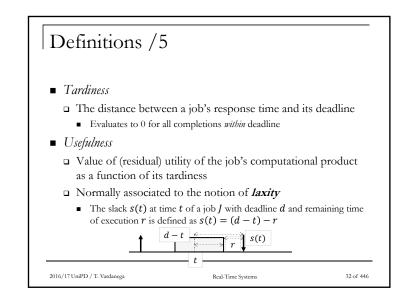


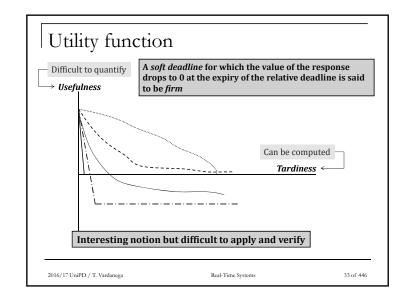


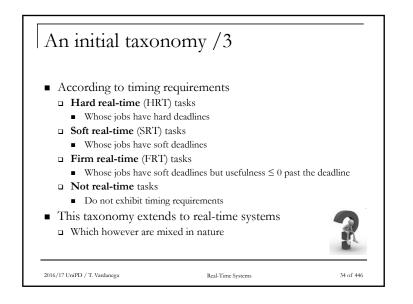


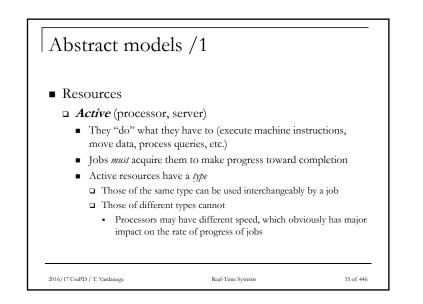


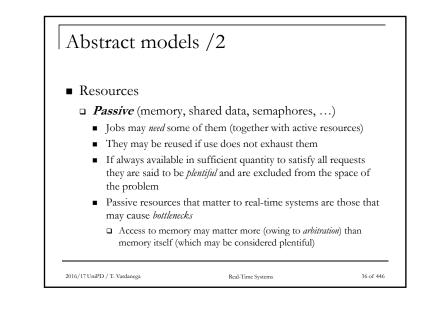


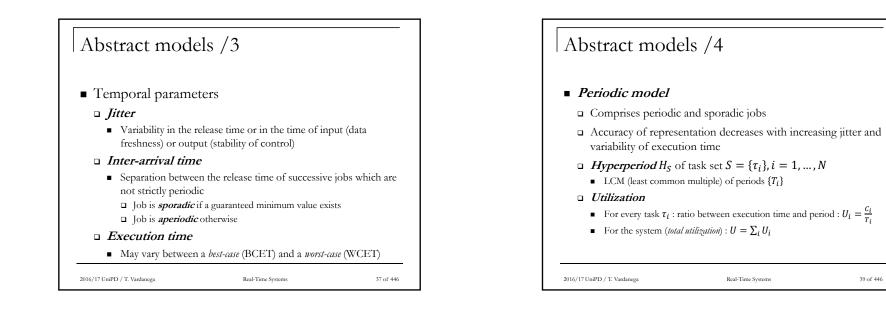


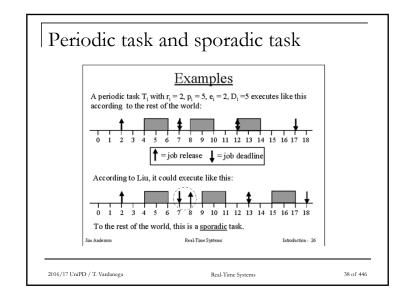


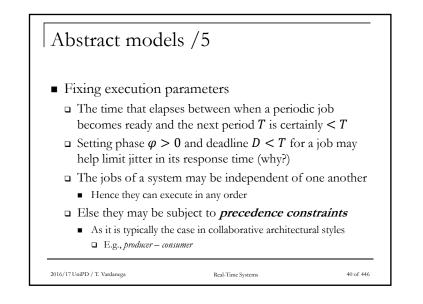


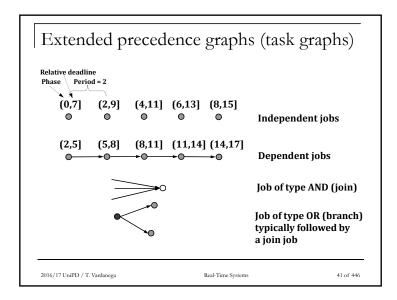


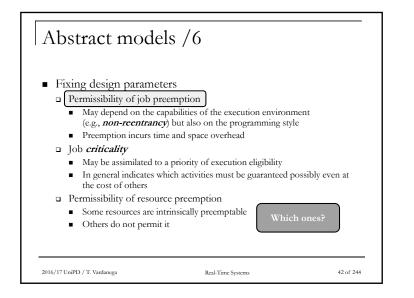


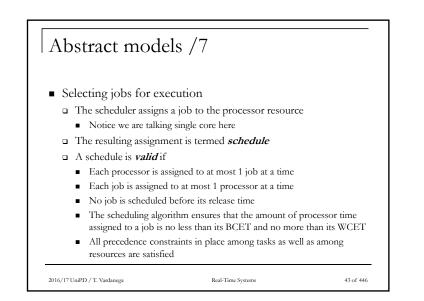


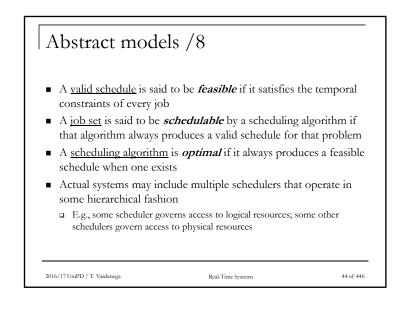


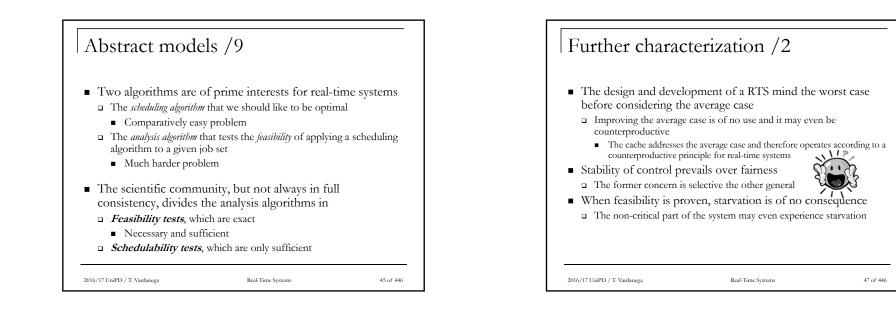












Further characterization /1		
	Time-Share Systems	Real-Time Systems
Capacity	High throughput	Ability to meet timing requirements: Schedulability
Responsiveness	Fast average response	Ensured worst-case latency
Overload	Fairness	Stability of critical part
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