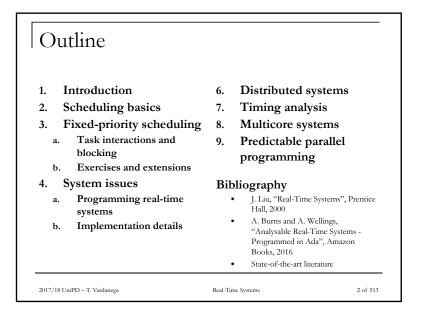
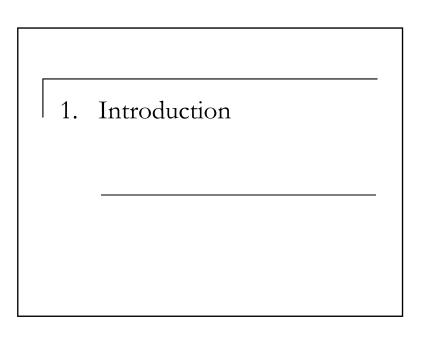
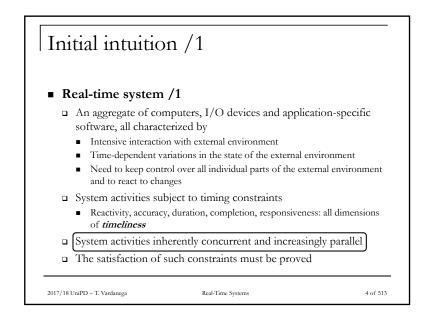
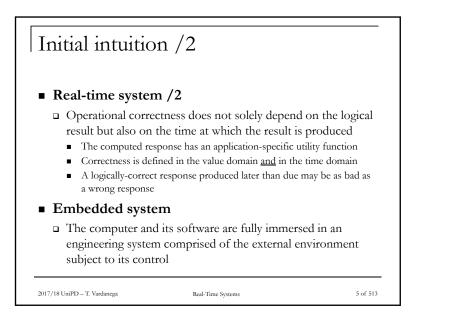
Real-Time Systems

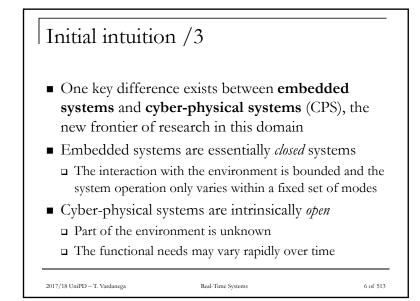
Academic Year 2017/18 Master Degree in Computer Science Department of Mathematics University of Padua Tullio Vardanega

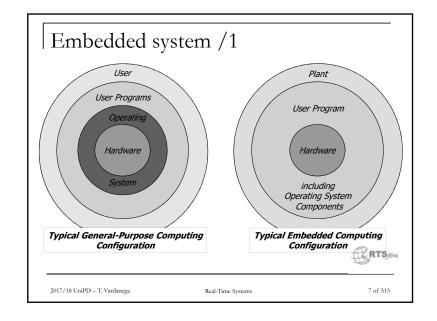


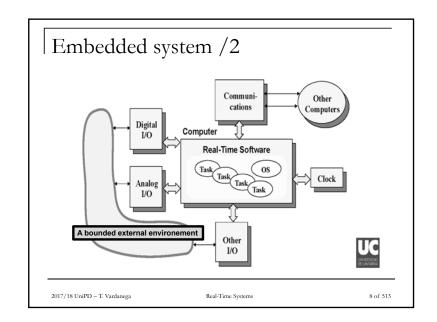


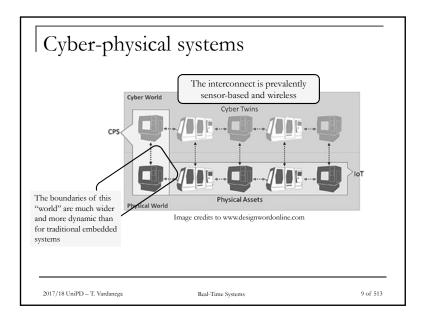


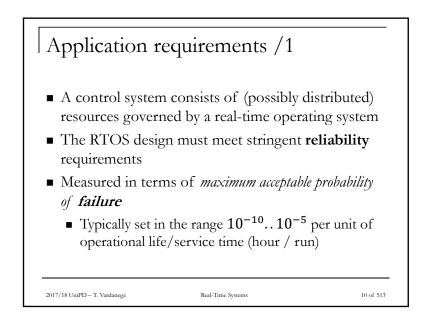


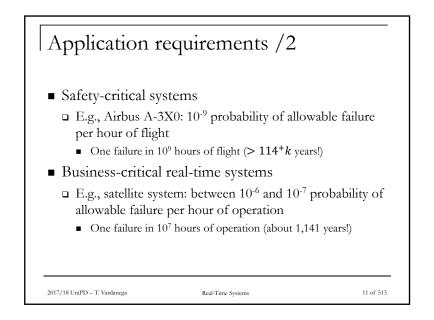


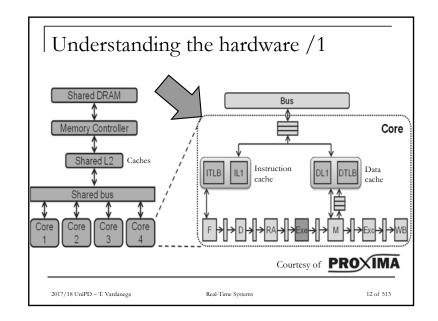


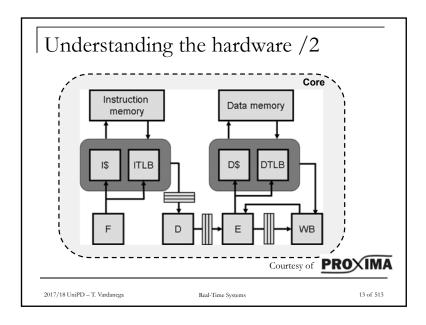


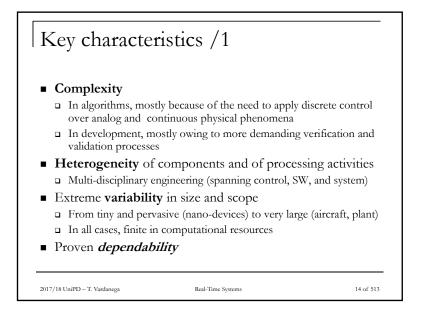


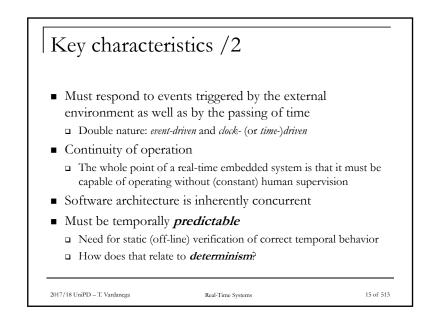


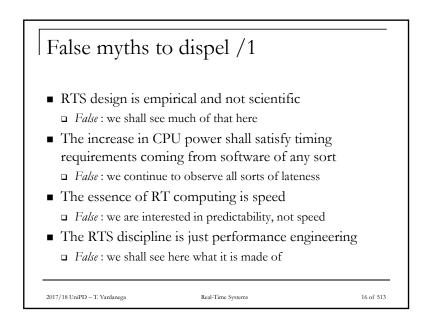


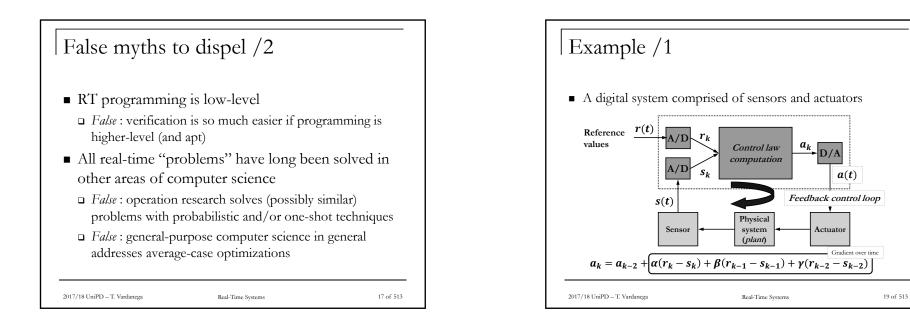


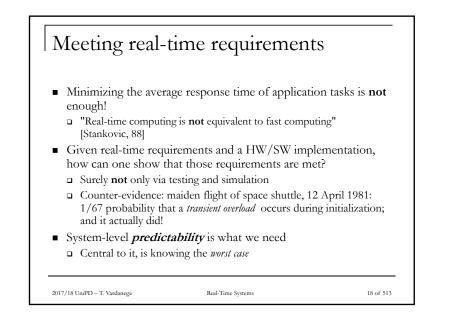


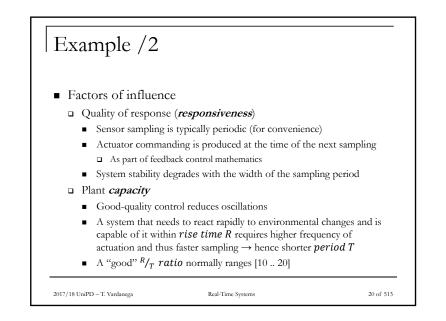


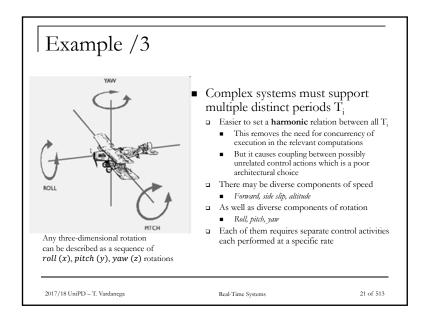


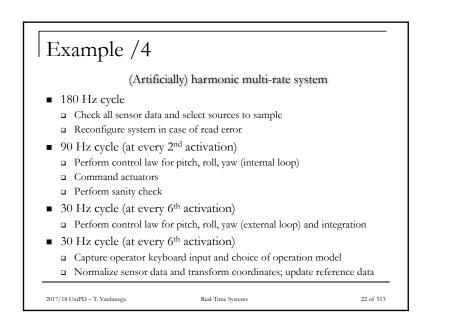


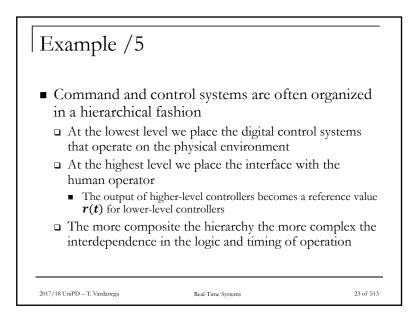


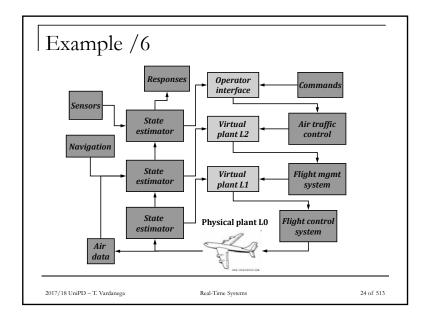


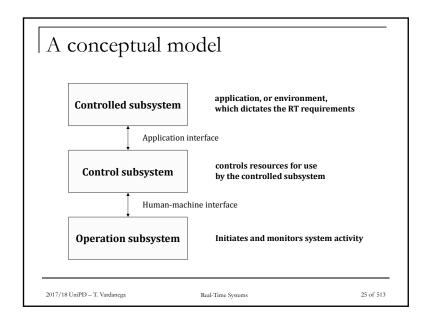


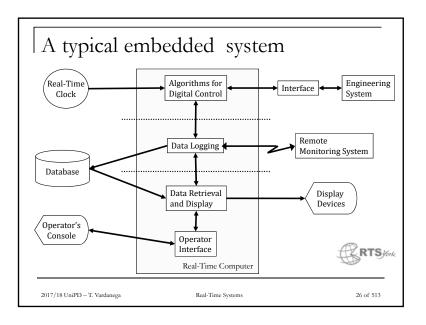


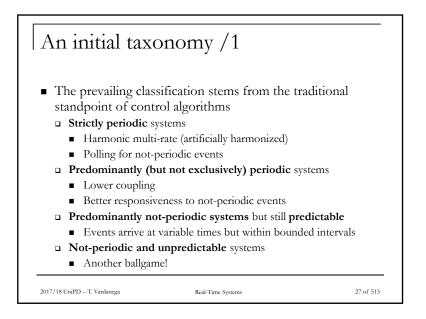


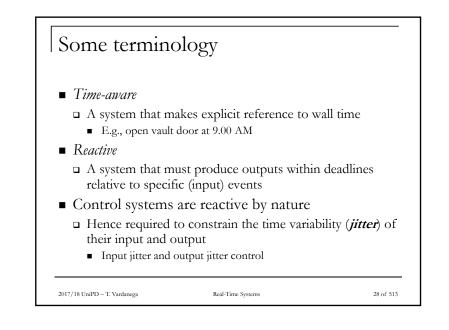


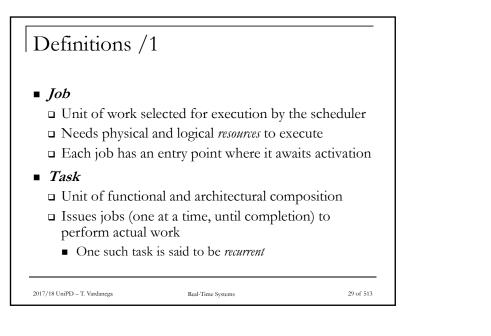


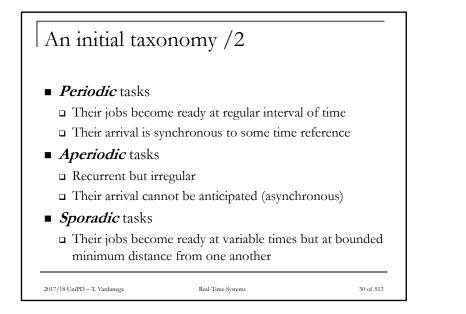


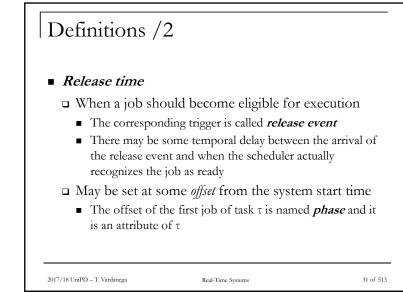


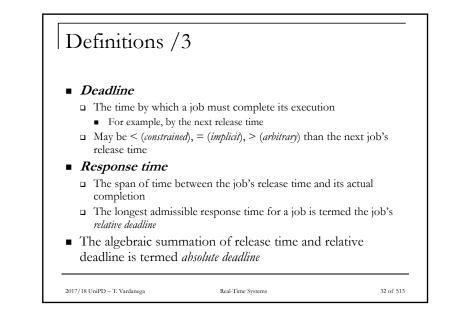


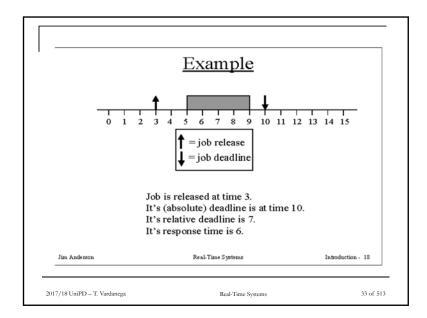


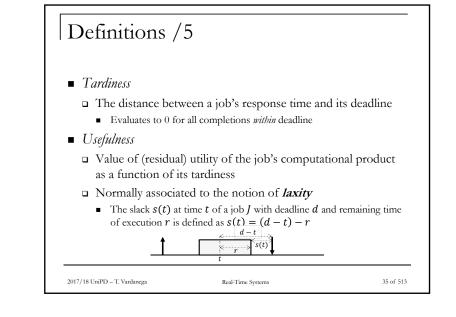


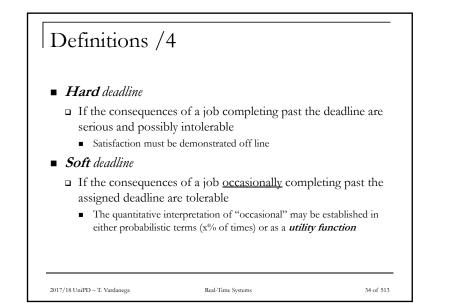


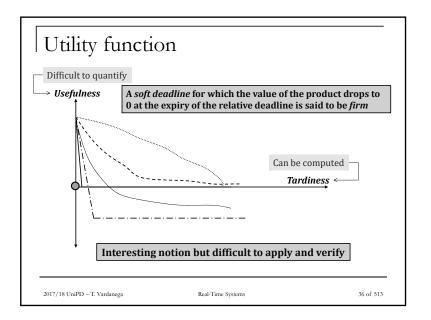


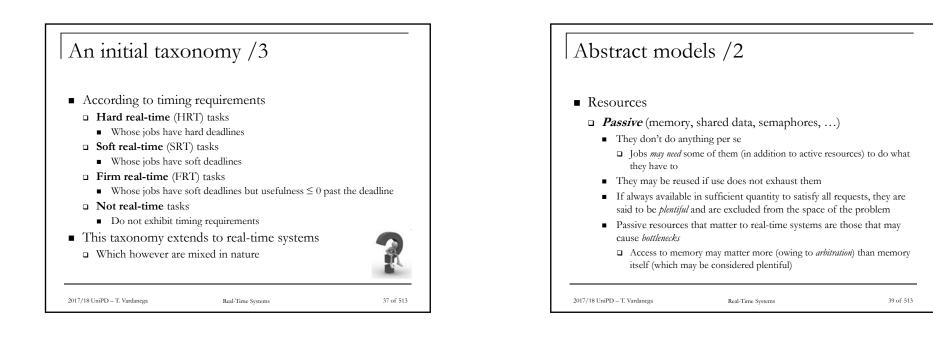


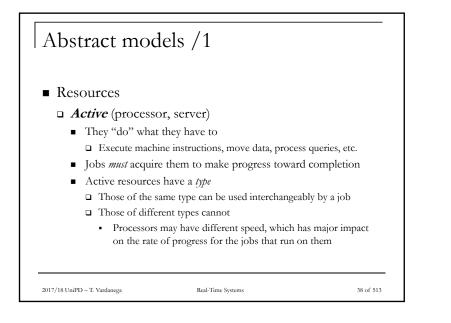


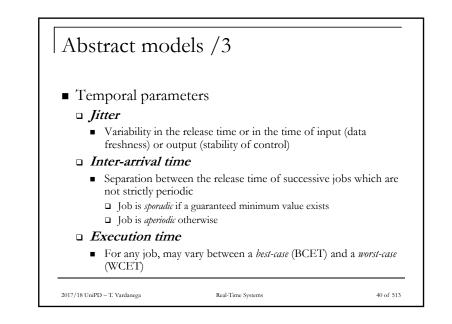


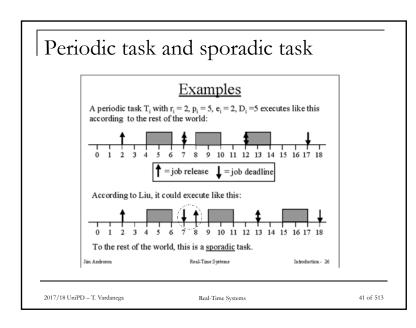


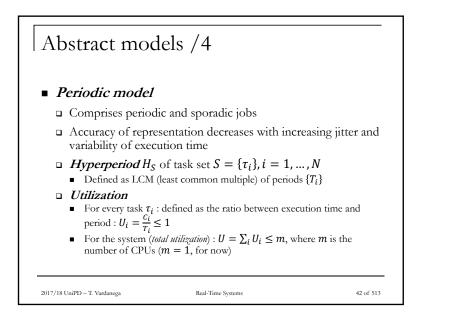


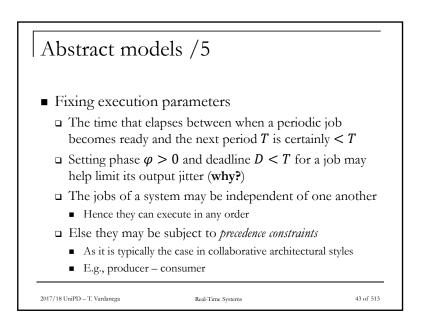


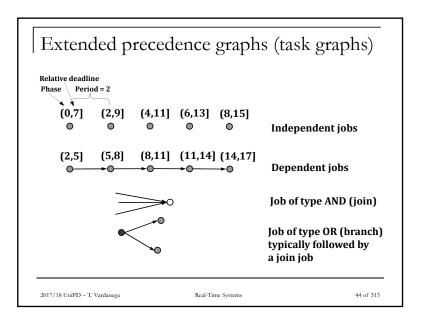




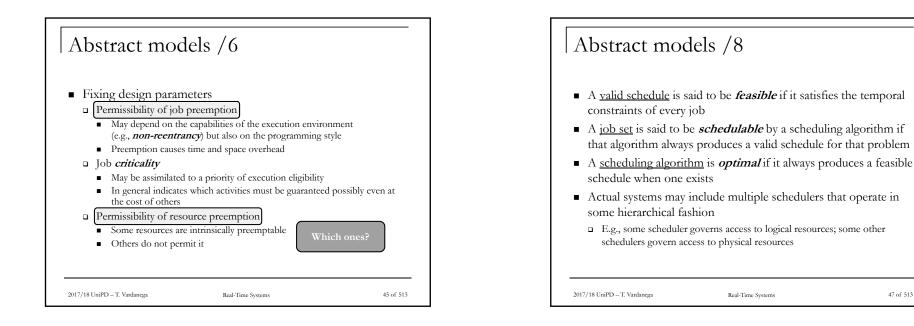


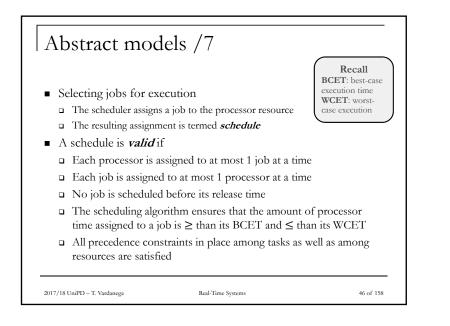


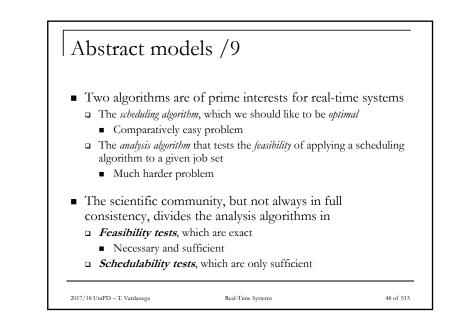


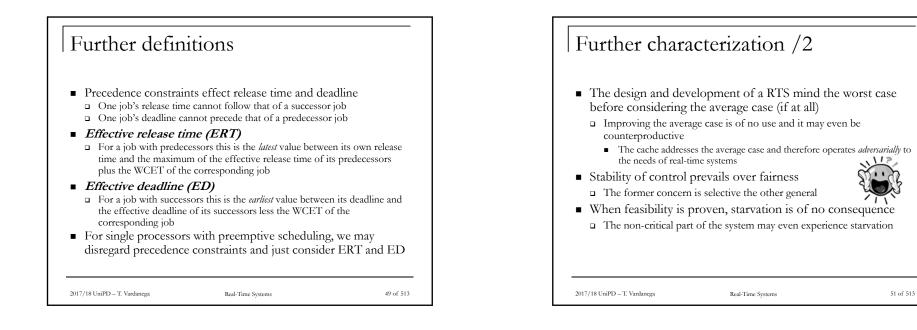


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	Time-Share Systems	Real-Time Systems
Capacity	High throughput	Ability to meet timing requirements: Schedulability
Responsiveness	Fast average response	Ensured worst-case latency
Overload	Fairness	Stability of critical part

